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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/686,121

10/14/2003

Brian L. Baskin

7614

7590

04/01/2005

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EXAMINER

RO, BENTSU

ART UNIT

PAPER NUMBER

2837

DATE MAILED: 04/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/686,121

Applicant(s)

BASKIN, BRIAN L.

Examiner

Bentsu Ro

Art Unit

2837

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 March 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-7 is/are allowed.
- 6) ☒ Claim(s) 8 is/are rejected.
- 7) ☒ Claim(s) 9 and 10 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## FINAL REJECTION

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Narita US Patent No. 6,614,208.

Claim 8 reads onto Narita's patent as follows:

A method of controlling a motor, said method comprising:	Narita Fig. 1 shows an apparatus and a method of a DC-to-DC converter for controlling a load 24 by using a half-bridge inverter (FETs Q1, Q2); the load 24 can be any load requiring a dc voltage, such as a motor; column 1, lines 12-13 states "DC-to-DC converters are used to obtain a specified DC voltage in a power circuit", a motor control circuit, of course, is a power circuit;
outputting an input dependent alternating signal, said alternating signal having a duty cycle that is a function of an input signal;	the voltage VSy is an input signal; the VSy voltage signal is inputted into an error amplifier 14; the error amplifier 14 compares the VSy signal with a reference signal Vref and generates an error output signal; the error output signal of the error amplifier is inputted to a pulse width modulation (PWM) circuit 16; the PWM circuit 16 outputs an alternating signal having a duty cycle, this alternating signal is a function of input signal VSy;
modulating said alternating signal with a second signal to output a modulated alternating signal,	Fig. 1 shows a differentiator 18, the output signal of the differentiator 18 is a second signal which is a time differentiating signal

	$dV_{sx}/dt$ ; the time differentiating signal (the second signal) modulates the alternating signal in a "dead time adjusting circuit" 20; the output of the dead time adjusting circuit 20 is a modulated alternating signal;  see the examiner's further explanations at the end of this comparison chart;
whereby said second signal is a <u>time derivative</u> function of a positive voltage supply signal;	the $V_{sx}$ signal at the source or drain of Q1 transistor (depends on the channel type of FET) is a positive voltage supply signal; this positive voltage supply signal $V_{sx}$ is time differentiated to generate a $dV_{sx}/dt$ , thus, the signal $dV_{sx}/dt$ is a time derivative function of the voltage signal $V_{sx}$ ;
transferring current to an output	the half bridge (Q1, Q2) transfers current to the load $Z_L$ ;
whereby said current is transferred from the voltage supply signal	the current to the load comes from the voltage $V_{sx}$ ; the voltage $V_{sx}$ is a positive voltage supply signal as explained previously;
and whereby the transfer of current to the output is a function of the modulated alternating signal. (currently amended)	the current and the voltage $V_{sx}$ is a function of modulated alternating signal because the transistors Q1 and Q2 are controlled by the dead time adjusting circuit.

The word "modulation" is defined as "Modulation causes a spectral shift in a signal...." by Lathi, see Lathi's "Signal Processing and Linear Systems", page 277, section 4.7, the first line after the subtitle "Application to Communications: Amplitude Modulation".

Narita Fig. 2 shows the structure of dead time adjustment circuit 20. The dead time adjustment circuit 20 includes a series of delay circuits 50, 52, these are RC delay

circuits to adjust and delay the output signal of the PWM circuit 16 to produce time delay signal of the PWM signal.

The time delay, according to Fourier transform, is a shift in frequency domain by an angle  $\exp(-j\omega t)$ , see Lathi's book, page 257, equation (4.37a).

The  $\exp(-j\omega t)$ , according to Euler's equation is

$$\exp(-j\omega t) = \cos(\omega t) - j \sin(\omega t)$$

which is an phase shift by the amount  $(-\omega t)$ . Thus, the time delay causes a spectral phase shift in the frequency domain. The time delay of PWM signal causes spectral phase shift of the PWM signal. Thus, the dead time adjusting circuit 20 is a spectral phase shift modulation circuit.

3. Claims 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 1-7 are allowable.

5. Applicant's arguments with respect to claim 8 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication should be directed to Bentsu Ro at telephone number 571 272-2072.

3/30/2005

  
Bentsu Ro  
Senior Examiner  
Art Unit 2837